WHAT IS CLAIMED IS:

1. A test system comprising:

a burn-in configuration register;

combinational logic operational in response to IC Die identification (ID) scan data and burn-in configuration register data to generate Die ID scan out signals;

means for generating memory built-in self-test (BIST) signals;

means for generating scan chain signals; and

exclusive-OR logic operational in response to the Die ID scan out signals, memory BIST signals, and scan chain signals to generate monitored output signals.

2. The test system according to claim 1, wherein the burn-in configuration register comprises:

a Die ID Scout Enable register;

a plurality of Scout Chain Enable registers, and

a Memory BIST status enable register.

3. The test system according to claim 1, wherein the combinational logic comprises AND logic.

4. A test system comprising:

means for configuring the test system;

means for generating Die identification (ID) scan out signals;

means for generating memory built-in self-test (BIST) signals;

means for generating scan chain signals; and

exclusive-OR logic operational in response to the Die ID scan out signals, memory BIST signals, and scan chain signals to generate monitored output signals.

5. The test system comprising according to claim 4, wherein the means for configuring the test system comprises a burn-in configuration register.

6. The test system comprising according to claim 5, wherein the means for generating Die ID scan out signals comprises combinational logic operational in response to IC Die identification (ID) scan out data and burn-in configuration register data to generate the Die ID scan out signals.

7. The test system according to claim 6, wherein the combinational logic comprises AND logic.

8. The test system according to claim 5, wherein the burn-in configuration register comprises:

a Die ID Scout Enable register; and

a plurality of Scout Chain Enable registers.

9. The test system according to claim 8, wherein the burn-in configuration register further comprises a memory built-in self-test (MBIST) Fail Enable register.

10. A method of observing integrated circuit (IC) failures during burn-in testing, the method comprising the steps of:

monitoring scan automatic test pattern generation (ATPG) and memory built-in self-test (BIST) patterns; and

selecting desired scan chain outputs and memory BIST status outputs to generate monitored IC output signals.

11. The method according to claim 10, wherein the step of monitoring scan ATPG and BIST patterns comprises monitoring die ID scan out signals, memory BIST signals, and scan chain signals.

12. The method according to claim 11, wherein the step of selecting desired scan chain outputs and memory BIST status outputs comprises combining the die ID scan out signals, memory BIST signals, and scan chain signals, and generating the monitored IC output signals there from.

13. The method according to claim 10, wherein the step of monitoring comprises the steps of:

configuring a burn-in configuration register;

combining IC Die identification (ID) scan out data and burn-in configuration register data to generate Die ID scan out signals; and

combining memory BIST fail/go-nogo status data and burn-in configuration register data to generate memory BIST signals.

14. The method according to claim 13, wherein the step of selecting desired scan chain outputs and memory BIST status outputs to generate monitored IC output signals comprises Exclusive-ORing the Die ID scan out signals, memory BIST signals, and scan chain signals to generate the monitored IC output signals there from.